

Appl. No. 09/654,253

Amendment dated September 15, 2006 filed with RCE

Response to Office Action of May 15, 2006

**Amendments to the Drawings**

The attached Sheet 2 of drawings includes changes to FIG. 2. This Sheet 2, which includes FIG. 2, replaces the original sheet 2 including FIG. 2. In FIG. 2, reference numeral 122 has been replaced with reference numeral 121 to resolve a duplicate reference numeral issue.

The attached Sheet 6 of drawings includes changes to FIG. 6. This Sheet 6, which includes FIG. 6, replaces the original sheet 6 including FIG. 6. In FIG. 6 near the top center of 152c, [Vg = -1] has been replaced with "Vd = -1" to resolve a clerical error.

Attachments: Replacement Sheets 2 and Sheet 6  
Annotated Sheet 2 and Sheet 6 Showing Changes

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**Remarks/Arguments**

**Brief Historical Background**

On November 17, 2004 a Final Office Action concerning the above identified Application was mailed to Applicants. On January 18, 2005 an After Final Amendment & Response including a Rule 1.131 Declaration signed by the Applicants and a Declaration by Applicant's Representative in Accordance with MPEP 608.01(p) was filed with the US Patent & Trademark Office. On March 1, 2005 an Advisory Action was mailed to Applicant's Representative by the US Patent & Trademark Office. On April 1, 2005 an Amendment, a further Rule 1.131 Declaration signed by the Applicants, and a Request for Continued Examination was filed. On June 28, 2005 an Office Action was mailed to Applicant's Representative by the US Patent & Trademark Office once again indicating that the Rule 1.131 Declaration was not effective to overcome a Zhang et al reference. On September 28, 2005 a response to the June 28, 2005 Office action was filed together with a further Rule 1.131 Declaration (Declaration under 37 CFR §1.131) signed by the Applicants. On December 16, 2005 another Office Action was mailed to Applicant's representative. On March 16, 2006 a response to the December 16, 2005 Office Action was filed. On May 15, 2006 a Final Office Action was mailed to the Applicant's representative. On July 14, 2006 a §116 Response to the Final Office action was filed and on August 10, 2006 an Advisory Action was mailed maintaining all rejections of all claims.

**Status and Summary of this response**

Claims 1-20 are pending and stand rejected on varying grounds under 35 U.S.C. 103(a).

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Claims 1 and 10 have been amended to further clarify the invention. Claim 11 has been canceled. Claims 5, 6, 9, 12, 15, 16, and 19 have been amended to resolve various informalities. Various paragraphs in the specification as well as FIG. 2 and FIG. 6 have been amended to resolve clerical errors. No new matter has been added by any amendment.

In view of the comments below, Applicant respectfully requests that the Examiner enter the proposed amendments, reconsider the present application including claims 1-10, and 12 - 20, withdraw the rejection of these claims, and move this application to allowance.

a) Sheet 2 and Sheet 6 consist respectively of FIG. 2 and FIG. 6. Each of these figures has been amended to correct clerical errors. Replacement sheets are being transmitted by facsimile together with this amendment. Formal replacement sheets are available to send to the US PTO when needed.

b) Claims 1-3 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, in view of Burrows, et al. (U.S. Patent No. 6,397,117 B1).

Claim 1 and claim 10 are independent claims with claims 2-3 dependent on claim 1.

Claims 1 and 10 have been amended to further clarify the invention by further specifying the claimed input fields to further distinguish the claimed invention from Michael et al and Burrows et al. Clearly the references of record do not show or suggest the newly cited features of claim 1

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or claim 10. For additional comments regarding differences between the claimed invention and these references, the Examiner is referred to July 14, 2006 §116 response.

Hence and in view of these discussions as well as the claim amendments, it is clear that Michael et al and Burrows et al do not show or suggest all features of either claim 1 or claim 10 or, at least by virtue of dependency, claim 2-3. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claim 1-3 and 10 under 35 U.S.C. 103(a) as being unpatentable over Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, in view of Burrows, et al. (U.S. Patent No. 6,397,117 B1).

c). Claims 4-6, 8-9 and 11-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State Circuits, Volume 27, Issue 2, February 1992, pages 154-166, and Burrows et al., U.S. Patent 6,397,117 B1 issued May 28, 2002, and filed May 28, 1998, in view of Applicants' admission.

Claim 11 has been canceled and thus this rejection of that claim is moot. Claims 4-6, and 8-9 are dependent on claim 1 and claims 12-20 are dependent on claim 10. As noted above claim 1 and 10 are clearly allowable over Michael et al and Burrows et al in any combination. Nothing in Applicants comments (alleged admission) provides the teachings that are missing from the combination of Michael et al and Burrows et al and thus claim 1 and claim 10 are allowable over this combination of references. Therefore, at least by virtue of dependency, claims 4-6, 8-9 and

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12-20 are likewise allowable over these references. For additional discussion concerning this rejection of these claims, the Examiner is referred to the July 14, 2006 §116 response.

Hence and in view of these discussions, it is clear that this combination of references does not show or suggest all features of any of claims 4-6, 8-9 and 12-20. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 4-6, 8-9 and 12-20 under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State Circuits, Volume 27, Issue 2, February 1992, pages 154-166, and Burrows et al., U.S. Patent 6,397,117 B1 issued May 28, 2002, and filed May 28, 1998, in view of Applicants' admission.

d) Claim 7 stands rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State Circuits, Volume 27, Issue 2, February 1992, pages 154-166, Burrows et al., U.S. Patent 6,397,117 B 1 issued May 28, 2002, and filed May 28, 1998, and Applicants' admission, in view of Hussey, U.S. Patent 5,826,269 issued October 20, 1998.

Claim 7 is dependent on claim 1 and claim 1 is believed to be allowable over Michael et al., Burrows et al., Applicant comments, and Hussey. Thus claim 7 at least by virtue of dependency is allowable over this combination of references. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claim 7 under 35 U.S.C.

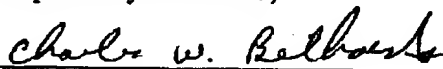
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103(a) based on Michael et al., "Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits", IEEE Journal of Solid-State circuits, Volume 27, Issue 2, February 1992, pages 154-166, Burrows et al., U.S. Patent 6,397,117 B 1 issued May 28, 2002, and filed May 28, 1998, and Applicants' comments, in view of Hussey, U.S. Patent 5,826,269 issued October 20, 1998.

Accordingly, Applicant respectfully submits that the claims clearly and patentably distinguish over all appropriately cited references of record and as such pending claims 1-10 and 12-20 are to be deemed allowable. Such allowance is hereby earnestly and respectfully solicited at an early date. If the Examiner has any suggestions or comments or questions, calls are welcomed at the phone number below.

Although it is not anticipated that any fees are due or payable, other than a Petition fee for 1 month time extension and RCE fee that are separately authorized and no other fees, are due or payable, the Commissioner is hereby authorized to charge any fees that may be required to Deposit Account No. 50-3435.

Respectfully submitted,

  
Charles W. Bethards  
Reg. No. 36,453

Attachments: Replacement Sheets 2 and Sheet 6  
Annotated Sheet 2 and Sheet 6 Showing Changes

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APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

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ANNOTATED SHEET SHOWING CHANGES

001050' E5245950

110
112
114
116
118

**MISMATCH CALCULATOR FOR DATA ENTRY**

☐ amos7lv

☐ MOS

☐ nlv

☐ Voltage Driven

☐ Create Data Entry Form

☐ View Related Plots

Model= amos7lv\_sps\_teg.udlib.rev0b

Calculate  email address:

**Single**

Vd: (V)

Vg: (V)

Vb: (V)

W: (cdr)

L: (cdr)

Temp (C):

**String**

**Range**

From  To

Cross Coupled? ☐ Center-to-Center  Sigmas(#):

☐ Show Mismatch Process Parameter Contributions

☐ Show Capacitances and Conductances

☐ Show Vdsat at  dB drop from peak Rout: Step Size=  V

120
121

130
150

158
100

**MISMATCH RESULTS**

W= 2	Vd= 2.5	X-Cpl= OFF
L= 2	Vg= 1	CTC= 0.0000
	Vb= 0	Sigma= 1
		Temp= 27

	Id MM (+/-)	Vg MM (+/-)
Total	2.7323%	4.9071mV
dl	0.0294	0.0442
dwox	0.0091	0.0193
gox	0.2070	0.4081
nsab	0.0118	0.0236
rsh	0.0000	0.0000
ubref	0.3572	0.7159
vfb	2.6715	4.7872
vcl	0.0026	0.0044
vtw	0.3956	0.6924

**MISMATCH NOTES**

Mismatch model based on Lot MB19188, wafer7 from C1SD

FIG. 2

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

ANNOTATED SHEET SHOWING CHANGES

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152c

MISMATCH RESULTS		
W= 1.0	Iref= 0.05	X-Cpl= OFF
L= 1	Vg= -1	CTC= 1.8000
Np=1	Vb= 0	Sigma= 1
Vd		Temp= 27

154c

	Id MM (+/-)	Vg MM (+/-)
Total	3.2060%	10.7680mV
dl	0.3814	1.2847
dwox	0.0701	0.2318
gox	0.3942	1.3314
nsub	0.2671	0.8961
rsh	0.0002	0.0009
ubref	1.0403	3.4466
vfb	2.9558	9.9430
vtl	0.2861	0.9631
vtw	0.0006	0.0019

157c

159c

155c

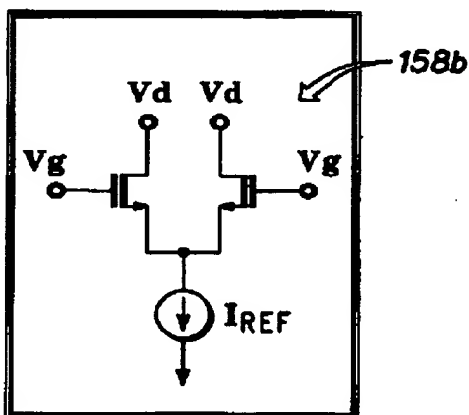


FIG. 6

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